REMARKS

Claims 1-3, 6-7, 9-10, 13, 15-16, and 19 are pending in the present application. Reconsideration and allowance of pending claims 1-3, 6-7, 9-10, 13, 15-16, and 19 in view of the following remarks are requested.

A. Rejection of Claims 1-3, 6, 9-10, and 15-16 under 35 USC §102(b)

The Examiner has rejected claims 1-3, 6, 9-10, and 15-16 under 35 USC §102(b) as being anticipated by U.S. patent number 6,190,975 to Kubo et al. ("Kubo"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 1, 9, and 15, is patentably distinguishable over Kubo.

In the Office Action dated March 3, 2005, the Examiner has ***finally rejected*** claims 1-3, 6, 9-10, and 15-16 pending in the application on the basis of a new ground of rejection and newly cited art "Silicon Processing for the VLSI Era" by Wolf, et al. (hereinafter "Wolf"). Applicant respectfully requests reconsideration and withdrawal of the finality of the rejection of the Office Action dated March 3, 2005. A good and sufficient reason why the present response is necessary and was not earlier presented is that an entirely new reference has been cited in the present final rejection dated March 3, 2005. 37 CFR §1.116(c). The new reference, i.e. Wolf, was for the first time brought to Applicant's attention by means of the present ***final rejection*** dated March 3, 2005. Since Wolf is a new reference upon which the Examiner has now relied, Applicant believes that

it would be manifestly unfair for the Patent Office not to consider Applicant's arguments which are necessitated due to the newly cited reference. As such, a good and sufficient reason exists, as required by 37 CFR §1.116(c), for considering Applicant's present response and withdrawing the finality of the present Office Action.

The present invention, as defined by amended independent claims 1 and 9, includes, among other things, a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where "said first gate dielectric and said first gate electrode are selected such that a difference between said second coefficient of thermal expansion and said first coefficient of thermal expansion causes an increase in carrier mobility in said FET." As disclosed in the present application, a FET includes a gate electrode layer situated over a gate dielectric layer, where the gate electrode layer and the gate dielectric layer are selected such that the gate electrode layer has a coefficient of thermal expansion ("CTE") that is higher than a CTE of the gate dielectric layer. As disclosed in the present application, as a wafer comprising the gate electrode and gate dielectric layers cools down after the gate electrode layer has been deposited at high temperature, the gate electrode layer decreases in size to a greater extent (i.e. shrinks more) than the gate dielectric layer. As disclosed in the present application, as a result, tensile strain is created in a channel situated underneath the gate dielectric, which advantageously increases carrier mobility in the FET.

As disclosed in the present application, in one embodiment, the FET is a PFET while gate dielectric and gate electrode layers are selected such that the gate dielectric layer has a CTE that is higher than the CTE of the gate electrode layer. In such embodiment, compressive strain is created in the channel underneath the gate dielectric layer, which increases carrier mobility in the PFET. Thus, by selecting gate electrode and gate dielectric layers of a gate stack to have appropriate respective coefficients of thermal expansion, the present invention achieves increased tensile strain in the channel of a FET. As a result, the present invention advantageously achieves increased carrier mobility in the FET, which results in increased FET performance.

In one embodiment, and referring to the drawings of the present application, gate electrode layer 114 and gate dielectric layer 116 are selected such that gate electrode layer 114 has a coefficient of thermal expansion ("CTE") that is higher than a CTE of gate dielectric layer 116. Thus, as a wafer comprising structure 100 cools down after gate electrode layer 114 has been deposited at high temperature, gate electrode layer 114 decreases in size to a greater extent (i.e. shrinks more) than gate dielectric layer 116. As a result, tensile strain is created in channel 112, which increases carrier mobility in FET 102. In one embodiment, FET 102 is a PFET while gate dielectric layer 116 and gate electrode layer 114 are selected such that gate dielectric layer 116 has a CTE that is higher than a CTE of gate electrode layer 114. In this embodiment, compressive strain is created in channel 112, which increases carrier mobility in the PFET.

In another exemplary embodiment, gate dielectric layer 216 is situated over channel 212 on top surface 218 of substrate 204. Also shown in Figure 2, gate electrode layer 220 is situated over gate dielectric layer 216 and may comprise, for example, polycrystalline silicon or other appropriate material. Further shown in Figure 2, gate electrode 222 is situated over gate electrode 220 and may comprise, for example, silicide or other appropriate material. In this embodiment, gate electrode layers 220 and 222 and gate dielectric layer 216 are selected such that gate electrode layer 222 has a CTE that is higher than a CTE of gate electrode layer 220 and the CTE of gate electrode layer 220 is higher than a CTE of gate dielectric layer 216.

Thus, as a wafer comprising structure 200 cools down after gate electrode layer 222 has been deposited at high temperature, gate electrode layer 222 decreases in size to a greater extent than gate electrode layer 220 and gate electrode layer 220 decreases in size to a greater extent than gate dielectric layer 216. As a result, tensile strain is created in channel 212, which increases carrier mobility in FET 202. In one embodiment, FET 202 is a PFET while gate dielectric layer 216 and gate electrode layers 220 and 222 are selected such that gate dielectric layer 216 has a CTE that is higher than a CTE of gate electrode layer 220 and the CTE of gate electrode layer 220 is higher than a CTE of gate electrode layer 222. In such embodiment, compressive strain is created in channel 212, which increases carrier mobility in the PFET.

Another exemplary embodiment is FET 302. FET 302 includes gate stack 306, which includes gate electrode layer 314 and gate dielectric layers 316 and 324, source

308, drain 310, and channel 312. Gate dielectric layer 316 is situated over channel 312 on top surface 318 of substrate 304 and may comprise silicon dioxide or other appropriate dielectric. Gate dielectric layer 324 is situated over gate dielectric layer 316 and may comprise silicon nitride or other appropriate dielectric. Gate electrode layer 314 is situated over gate dielectric 324. Gate electrode layer 314 can be deposited over gate dielectric layer 324 at high temperature utilizing a CVD process or other appropriate processes.

In this embodiment, gate electrode layer 314 and gate dielectric layers 316 and 324 are selected such that gate electrode layer 314 has a higher CTE than a CTE of gate dielectric layer 324 and gate dielectric layer 324 has a higher CTE than a CTE of gate dielectric layer 316. Thus, as a wafer comprising structure 300 cools down after gate electrode layer 314 has been deposited at high temperature, gate electrode layer 314 is reduced in size to a greater extent than gate dielectric layer 324 and gate dielectric layer 324 is reduced in size to a greater extent than gate dielectric layer 316. As a result, tensile strain is created in channel 312, which increases carrier mobility in FET 302. In one embodiment, FET 302 is a PFET while gate dielectric layers 316 and 324 and gate electrode layer 314 are selected such that gate dielectric layer 316 has a CTE that is higher than a CTE of gate dielectric layer 324 and gate dielectric layer 324 has a higher CTE than a CTE of gate electrode layer 314. In such embodiment, compressive strain is created in channel 312, which increases carrier mobility in the PFET.

In contrast, Kubo does not teach, disclose, or suggest a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where "said first gate dielectric and said first gate electrode are selected such that a difference between said second coefficient of thermal expansion and said first coefficient of thermal expansion causes an increase in carrier mobility in said FET." Kubo specifically discloses an NMOS transistor including SiGeC layer 14n, gate insulating layer 19n, and gate electrode 18n, where gate electrode 18n is situated over gate insulating layer 19n and gate insulating layer 19n is situated over SiGeC layer 14n, which serves as channel. See, for example, column 9, lines 7-23 and Figure 1 of Kubo. In Kubo, the composition rates of the respective elements in SiGeC layer 14n are set such that SiGeC layer 14n and Si layer 13n immediately therebelow are fitted in lattice for each other. See, for example, column 8, lines 57-61 and Figure 1 of Kubo.

In Kubo, in SiGeC layer 14n, the electron mobility is higher than in the Si layer, thus increasing the operational speed of the NMOS transistor. See, for example, Kubo, column 9, lines 4-6. However, Kubo fails to teach, disclose, or suggest a first gate dielectric and a first gate electrode being selected such that a difference between the second coefficient of thermal expansion of the first gate electrode and the first coefficient of thermal expansion of the first gate dielectric causes an increase in carrier mobility in the FET. Furthermore, Kubo fails to even mention a coefficient of thermal expansion.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by amended independent claims 1 and 9, is not taught, disclosed, or suggested by Kubo. Thus, amended independent claims 1 and 9 are patentably distinguishable over Kubo. As such, the claims 2-3 and 6-7 depending from amended independent claim 1 and claims 10 and 13 depending from amended independent claim 9 are, *a fortiori*, also patentably distinguishable over Kubo for at least the reasons presented above and also for additional limitations contained in each dependent claim. Further, the cited portions of Wolf are merely directed to properties of silica glass and silicon, and there is no motivation disclosed either in Wolf or Kubo to combine the two references to achieve an increased carrier mobility FET as taught and claimed by the present invention.

The present invention, as defined by amended independent claim 15, includes, among other things, a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where "said first gate dielectric and said first gate electrode are selected such that a difference between said second coefficient of thermal expansion and said first coefficient of thermal expansion causes a strain in said channel, said strain causing an increase in carrier mobility in said FET." Amended independent claim 15 recites similar limitations as amended independent claims 1 and 9 discussed above. Thus, for similar reasons as discussed above, amended independent claim 15 is also patentably distinguishable over Kubo. Thus claims 16 and 19 depending from amended independent claim 15 are, *a fortiori*, also patentably distinguishable over Kubo for at least the reasons presented

above and also for additional limitations contained in each dependent claim. Moreover, as stated above, the cited portions of Wolf are merely directed to properties of silica glass and silicon, and there is no motivation disclosed either in Wolf or Kubo to combine the two references to achieve an increased carrier mobility FET as taught and claimed by the present invention.

B. Rejection of Claims 7, 13, and 19 under 35 USC §103(a)

The Examiner has rejected claims 7, 13, and 19 under 35 USC §103(a) as being unpatentable over Kubo. However, as discussed above, amended independent claims 1, 9, and 15 are patentably distinguishable over Kubo. Thus, claim 7 depending from amended independent claim 1, claim 13 depending from amended independent claim 9, and claim 19 depending from amended independent claim 15 are, *a fortiori*, also patentably distinguishable over Kubo for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1, 9, and 15 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-3, 6-7, 9-10, 13, 15-16, and 19 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, withdrawal of the finality of

the present rejection and an early allowance of claims 1-3, 6-7, 9-10, 13, 15-16, and 19 pending in the present application are respectfully requested.

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Respectfully Submitted,
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